Min Wei

kinling9

vmin6810@gmail.com

Education

Sep 2021 – Jun 2026 **Ph.D., Fudan University** Integrated Circuit and System Design.
Research Interests:

- *Very Large-Scale Integration (VLSI) Placement Algorithms;*
- *Physical aware Synthesis Flow ;*
- *Timing Prediction and Static Timing Analysis.*

Sep 2017 – Jun 2021 **B.S., Fudan University** Microelectronic Science and Engineering.
Thesis Title: *Timing-Driven Detailed Placement for large-scale heterogeneous FPGAs*.

Employment

Jul 2026 – Present **Senior Engineer,** Shanghai LEDA Technology Co., Ltd.
Agentic EDA: Building an industrial-grade RTL-to-GDS agent that drives the implementation flow end to end with almost no human intervention, targeting better PPA and lower power.
LLM Infrastructure: Local deployment of large language models, inference-efficiency optimization for coding-agent workloads, and the setup and management of LLM gateways.

Internship Experience

Oct 2024 – Aug 2025 **Software Development & Product Application Intern,** Shanghai LEDA Software Technology
Responsibilities: Participated in the localization substitution and optimization of EDA tools in multiple partitions (e.g., XPU, GPU) on SMIC process nodes. Responsible for building the workflow and optimizing PPA results for the Pre-CTS stage using domestic EDA tools.

Oct 2023 – Sep 2024 **Software Development Intern,** Shanghai LEDA Software Technology
Responsibilities: Developed a timing prediction tool using placement results to bridge logic synthesis and physical design. This allowed for re-synthesis flow, which optimized the netlist and placement for better performance.

Jul 2021 – Sep 2023 **Software Development Intern,** Shanghai LEDA Software Technology
Responsibilities: Optimized wirelength and prevented timing violations using analytical placement methods. Developed and integrated custom algorithms into domestic EDA tools, achieving superior PPA results on industrial benchmarks.
Publications: *Electrostatics-based analytical global placement for timing optimization* [2]; *An Analytical Placement Algorithm with Routing topology Optimization* [4]

Internship Experience (continued)

Sep 2020 – Jun 2021 — **Software Development Intern,** Shanghai Fudan Microelectronics Group
Responsibilities: Contributed to the development of EDA tools for FPGA design. Assisted in developing a detailed placement tool for FPGAs, where the related algorithms effectively improved the timing quality of FPGA layouts.

Research Publications

1. Y. Chen, Z. Cai, **M. Wei**, Z. Lin, J. Chen, "Global and local attention-based inception u-net for static ir drop prediction," in *2024 IEEE 42nd International Conference on Computer Design (ICCD)*, IEEE, 2024, pp. 673–680.
2. Z. Lin, **M. Wei**, Y. Chen, P. Zou, J. Chen, Y.-W. Chang, "Electrostatics-based analytical global placement for timing optimization," in *2024 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, IEEE, 2024, pp. 1–6.
3. X. Tong, "Layout-level hardware trojan prevention in the context of physical design," in *Proceedings of the 43rd IEEE/ACM International Conference on Computer-Aided Design*, 2024, pp. 1–9.
4. **M. Wei**, X. Tong, Z. Cai, P. Zou, Z. Lin, J. Chen, "An analytical placement algorithm with routing topology optimization," in *2024 29th Asia and South Pacific Design Automation Conference (ASP-DAC)*, IEEE, 2024, pp. 294–299.
5. **M. Wei**, "Analytical placement with 3d poisson's equation and admm-based optimization for large-scale 2.5 d heterogeneous fpgas," *ACM Transactions on Design Automation of Electronic Systems*, vol. 28, no. 5, pp. 1–24, 2023.

Skills

Languages	CET-6, proficient in technical document reading and writing, capable of daily communication and academic discussions
Coding	C/C++, Python, Tcl, Shell (Bash, CShell), LaTeX, …
EDA Tools	Cadence Innovus, Synopsys Design Compiler, Mentor Graphics ModelSim, Cadence Virtuoso, Synopsys VCS, Xilinx Vivado
Design Languages	Verilog, SDC, DEF/LEF, Liberty, SystemVerilog, UVM
Misc.	Git, (Neo)Vim, CMake, Linux, Docker, Agile Development Workflow

Additional Experiences

Major Competitions and Awards

2023 — **First Place**, ISPD 2023 Contest.
Topic: *Security Closure of Physical Layouts*
Contribution: Built a full chip implementation flow using Cadence Innovus tool, achieving co-optimization of PPA metrics and layout security.
Publications: *Layout-level Hardware Trojan Prevention in the Context of Physical Design* [3]

Additional Experiences (continued)

Other Competitions and Awards

2021 **First Prize**, 4th China Postgraduate IC Innovation Competition.

Third Prize, 3rd EDA Elite Challenge Contest.

2022 **Honorable Mention**, 2022 CAD Contest @ICCAD.

2023 **Second Place**, 2023 CAD Contest @ICCAD.

First Prize, 5th EDA Elite Challenge Contest.

China Education Development Foundation Endeavor Scholarship—Integrated Circuit

2024 **Third Place**, ISPD 2024 Contest.